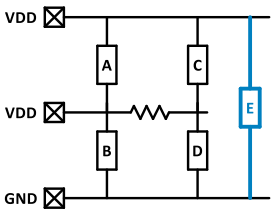
0.75V ESD power protection – TSMC 3nm Enhanced

ESD Device – Type E

ESD power protection

Cell name: ZZ_075_V_Rail_PS_0



The ESD clamp is designed to provide 8kV HBM protection for 0.75 V Analog and Core domain using 0.75V FinFet transistors in TSMC N3E process.

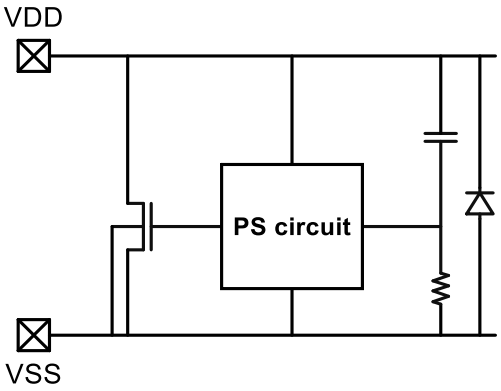
This clamp is selected for the protection of the following specific application:

0.75V Power domain using 0.75V FinFet transistors.

Features:

- Efficient ESD power protection
  - Up to ± 8 kV Human Body Model (HBM)
  - Up to ± 1 kV Charged Device Model (CDM)
  - Latch-Up safe

Circuit schematic:



MAXIMUM RATINGS

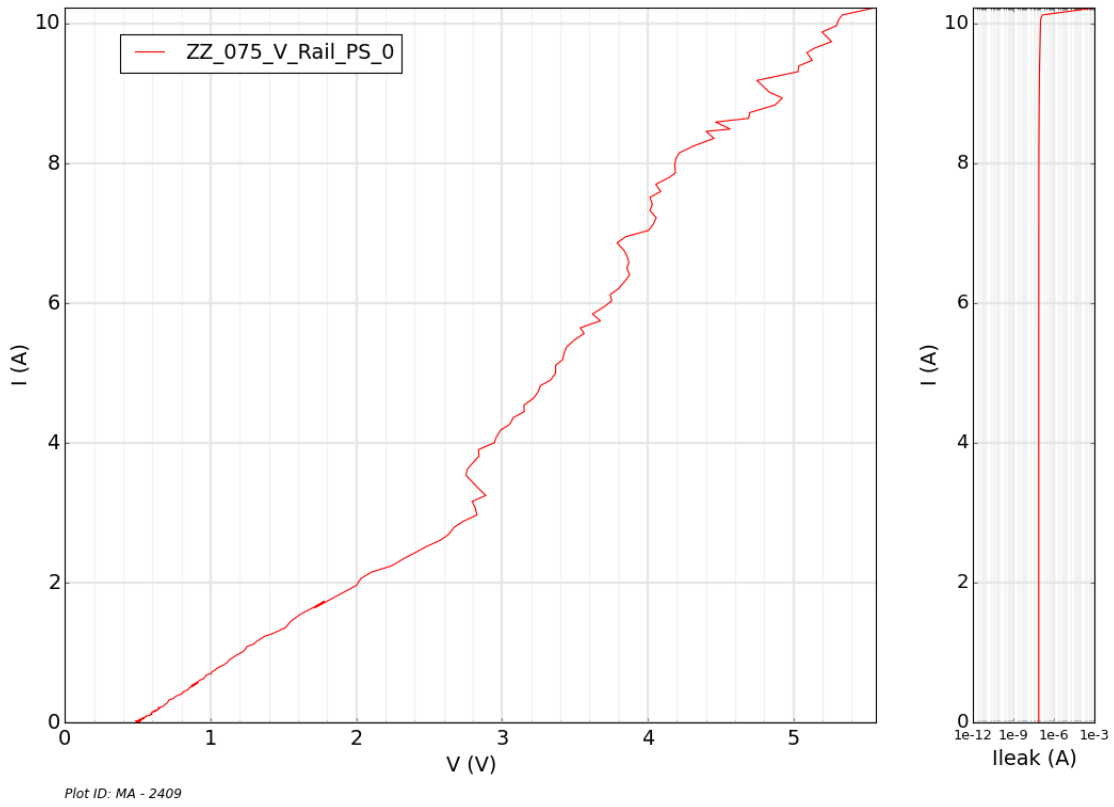
Rating	Symbol	Value		Unit
		Min	Max	
Supply Voltage Range (DC)	V_{DD}	-0.3	1.32	V
Max. Operating Temperature		125		°C

Stresses exceeding these maximum ratings may damage the device. Functional operation above the recommended operating conditions is not implied. Extended exposure to stresses above the recommended operating conditions may affect device reliability.
The provided golden cell is designed for these maximum ratings/specifications. If the desired specification level differs, the golden cell has to be scaled up or down by using the Sofics implementation/scaling guidelines to remain a robust and effective ESD protection for the different specifications.

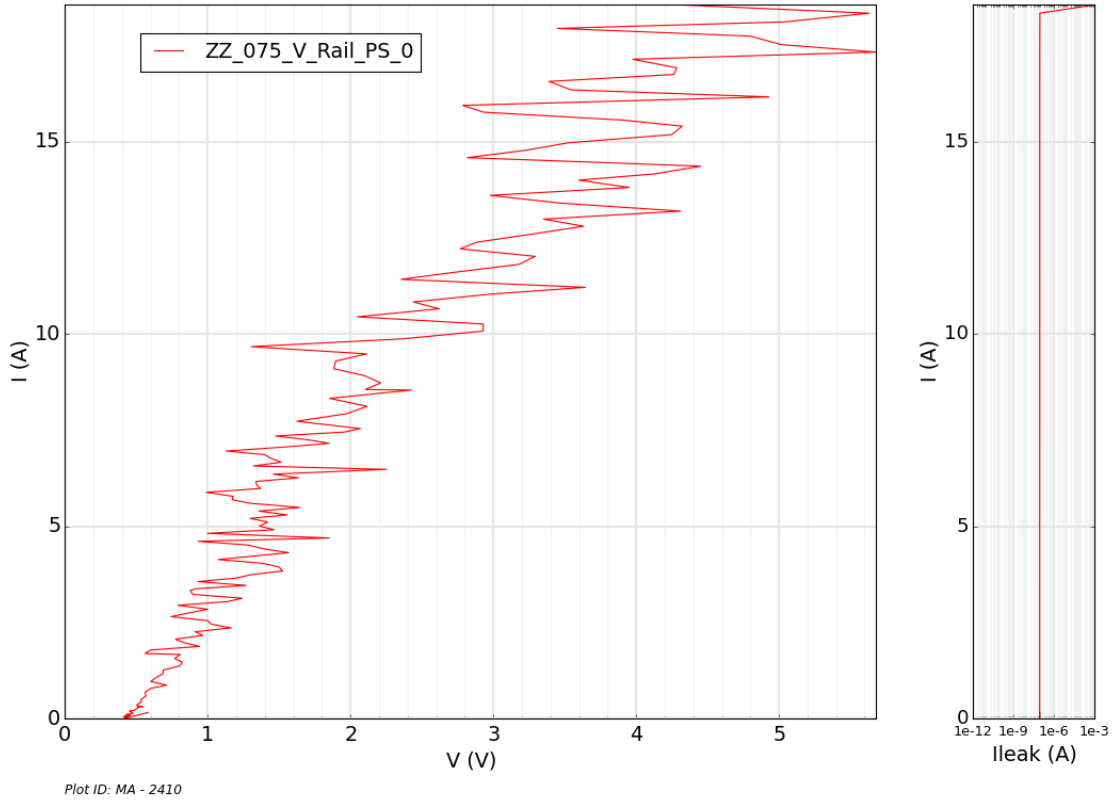
ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C unless stated otherwise)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	- 0.3	0.75	1.08	V
Trigger Voltage	V_{t1}	-	0.5	-	V
Breakdown Voltage	V_{t2}	-	5.3	-	V
Maximum Current	I_{max}	-	> 10	-	A
On-Resistance	R_{on}	0.4	0.48	0.6	Ohm
Reverse Voltage	V_{rev}	-	1	-	V
Maximum Current of Reverse Diode	$I_{max,RD}$	-	> 10	-	A
On-Resistance of Reverse Diode	R_{on}	0.4	0.48	0.6	Ohm
Operating Temperature Range	T_{op}	-40	-	+125	°C
HBM – Human Body Model		-2 till -8	-	+2 till +8	kV
CDM – Charged Device Model		-250 till -1000	-	+250 till +1000	V

TLP I-V

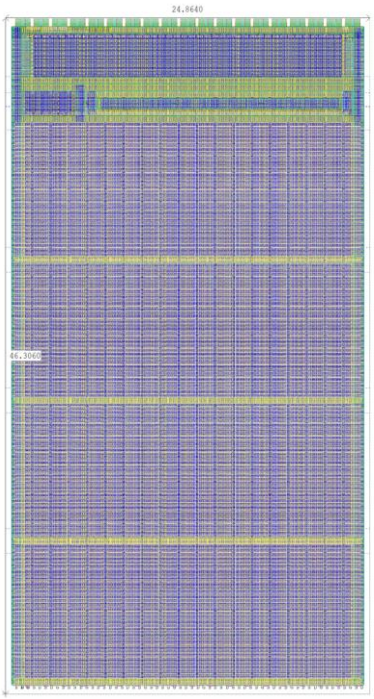


VF-TLP I-V


ZZ_075_V_Rail_PS_0
I (A)
V (V)
0
5
10
15
0
1
2
3
4
5
Plot ID: MA - 2410
I (A)
Ileak (A)
1e-12
1e-9
1e-6
1e-3

LAYOUT/DIMENSIONS: ZZ_075_V_Rail_PS_0

- Process: TSMC 3nm FinFet Enhanced
- Used Metals: 1P15M_1Xa_h_1Xb_v_1Xc_h_1Xd_v_1Ya_h_1Yb_v_4Y_hvhv_2Yy2Z
- Required Special Layer: /
- Area:
  - 8kV: 1151.3µm² (24.864µm x 46.306µm)
  - 6kV: 911.9µm² (24.864µm x 36.674µm)
  - 4kV: 680.3µm² (24.864µm x 27.361µm)
  - 2kV: 432.9µm² (24.864µm x 17.410µm)



CONNECTION GUIDELINES

- 2 paths are required to be connected:
  - VDD: power, highest potential of domain to be protected
  - VSS: ground, lowest potential of domain to be protected
- All buses in the clamp can be used as feed-through buses.
- P+ guardbands are connected to VSS (ESD clamp is not isolated from substrate).

Respect the repetition rate/maximum allowed bus resistance when connecting with a power clamp in order to ensure the ESD robustness!
The maximum bus resistance should not exceed 0.8 Ω between 2 power clamps.