Optimized Local I/O ESD Protection in FinFET Technology for 2.5D and 3D hybrid integration

Bart Keppens, Johan Van der Borght

Sofics, 32 Sint-Godelievestraat, B-9880 Aalter, Belgium,
phone: ++32-9-21-68-333; fax: ++32-9-3-746-846; e-mail: bkeppens@sofics.com

Abstract: Semiconductor companies using 2.5D and 3D hybrid integration need to consider Electrostatic Discharge (ESD) protection early in the design, even for die-2-die interfaces that remain inside the package. There are several challenges but also opportunities. The use of a local ESD protection clamp at the TSV offers more robustness, higher performance, more flexibility, all in a strongly reduced silicon footprint.

I. Introduction

A growing number of semiconductor applications are turning to 2.5D and 3D integration for various reasons. Integrating multiple dies in a single package can (1) reduce total power consumption, (2) reduce required PCB area, (3) enhance performance (higher communication speed) and (4) it can speed up development cycles. It also (5) makes it harder for a competitor to copy a chip design/functionality. Finally, (6) it allows to use the most optimal process technology for each function.

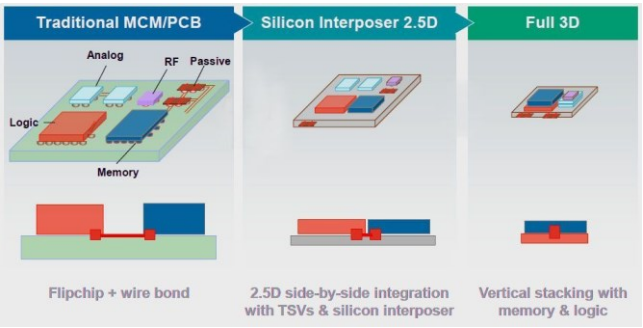

Figure 1: From traditional PCB or MCM approach (left), over 2.5D (middle) to full 3D stacked (right) approach.

Whatever the reason for hybrid integration, it is important to consider Electrostatic Discharge (ESD) protection early in the design phase. In the case of packages with a single die, the ESD challenges and solutions have been studied for decades. With the advance of 2.5D and 3D integration, there are new challenges but also opportunities.

II. Hybrid assembly

There are already quite some applications that use such hybrid assembly techniques. Chip makers have for instance combined a logic controller chip together with a Microelectromechanical systems (MEMS) in one package. This approach has been used for accelerometers/gyroscope and other sensor products to reduce the size and volume of the product. Other companies have developed silicon-based oscillators to improve the accuracy and flexibility of crystal oscillators. In that case the MEMS is the heart of the oscillator and the logic chip is used to add flexibility like setting different frequencies.

One of the typical 3D examples is the Hybrid Memory Cube (HMC) - Figure 2. In this architecture several DRAM chips are stacked on top of a logic layer. The DRAM chips need a special DRAM process technology (Deep-trench storage capacitor) while the logic layer is built with the most advanced FinFET node. The signals to/from the DRAM layers are sent to the other layers with so-called Through-Silicon Vias (TSV). This has several advantages. The shorter connections allow faster memory access and the 3D stacking also reduces the size/volume of the entire circuit.

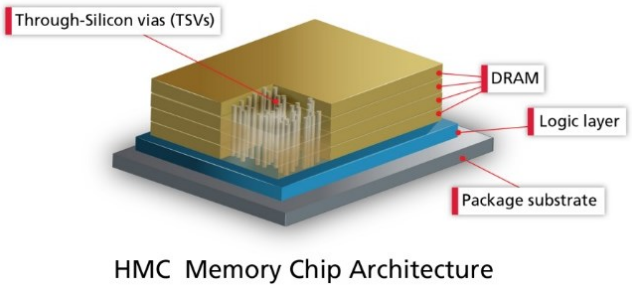

Figure 2: Hybrid Memory Chip or Cube architecture. Through-Silicon via's are used for the connections between the logic layer and the DRAM layers.

The discussion below about ESD protection is based on co-packaged projects for silicon-based timing products, SerDes on a chiplet and support for improving ESD of a Hybrid Memory Cube. Customized ESD solution libraries (90nm and 65nm CMOS) have been delivered to a CMOS imager company. That company is using 3D stacking to combine a logic chip and the pixel/sensor chip.

ESD protection devices with ultra-low parasitic capacitance have been delivered to more than 15 projects for Silicon Photonics datacenter solutions. In these applications a logic controller, laser and optical die are connected in a single assembly.

III. Influence on ESD protection

For the discussion on ESD protection we define 2 types of chip interfaces.

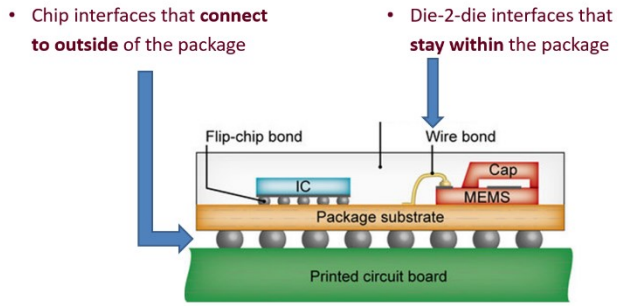

Figure 3: Comparison between 2 types of interfaces: (1) connecting outside of the package to PCB traces and (2) connecting dies inside the same package.

1. Chip interfaces that connect outside of the package. These could be bond wires, balls/bumps.

2. Chip interfaces that stay within the package. The connections between different dies inside the package are sometimes referred to as 'die-2-die' links. They can consist of wire bonds, flip-chip bonds, through-silicon-via's (TSV) for 3D stacked dies.

Below the 3 different aspects (ESD robustness, signal voltage conditions and layout) are discussed for both chip interface options.

III. A ESD robustness

For the first type of interfaces, IC designers have to use the conventional ESD robustness requirements. For most applications that means at least 2kV HBM and about 300 to 500V CDM. There are various applications with special ESD requirements but that is not the scope of this paper. For instance, it is quite common to reduce the ESD level (to 1kV HBM, 250V CDM) for wireless interfaces or for high-speed communication interfaces. The on-chip ESD protection devices are required to protect against ESD events on the exposed package pins during assembly, transport or testing of the IC product.

On the other hand, for chip interfaces that stay inside the package the ESD robustness requirement can be drastically reduced. Since the connections are not exposed once the IC package is sealed, the likelihood of ESD stress on those lines during IC transport, PCB assembly is strongly reduced [1]. The on-chip ESD devices cannot be completely removed though. ESD events could still occur during the assembly of the different dies inside the package. But such assembly is typically performed under very (ESD) safe/controlled conditions. Actually, the assembly supplier will provide guidelines on minimum ESD requirements. Additionally the die-2-die links can be damaged during CDM stress. They are somewhat similar to interdomain interfaces in large SoC's.

For instance, from discussions with customers in several co-packaged projects we learned that the HBM robustness level for die-2-die interfaces in silicon photonics applications is reduced to 200V or even 100V. For 112Gbps SerDes chiplets the ESD requirement was set at just 35V CDM.

III. B Interface signal voltage

There are always exceptions but for the majority of chip interfaces that connect outside of the package, IC designers rely on the standard IO library (e.g. 1.8V, 2.5V, 3.3V).

Output drivers need to use a high enough voltage and provide large output drive current to ensure the signal can reach the other chips on the PCB and charge up the (parasitic) loading capacitance. Usually the functional I/O circuits are built with high voltage (1.8V, 2.5V or 3.3V), thick oxide transistors. Typical exceptions are (again) wireless interfaces or high-speed communication lines.

Die-2-die interfaces that stay inside the package on the other hand, do not need high voltage or high drive current capability. The output drivers can be made smaller and can be designed using thin oxide transistors. These transistors are faster but are also more sensitive to ESD events. Typical foundry provided GPIO libraries do not have digital or analog I/O cells for these low voltage cases. More effective ESD clamps are needed to protect the sensitive thin oxide transistors and to enable low voltage (1.2V, 1.0V or even lower) operation.

Of course, there are cases where the voltage is actually higher. Some of the applications that involve a combination of logic CMOS chips and MEMS actually need a higher output voltage like 5V or 10V, also beyond the foundry I/O options.

III. C Layout aspects

Finally, there are several differences for the actual I/O and ESD clamp layout.

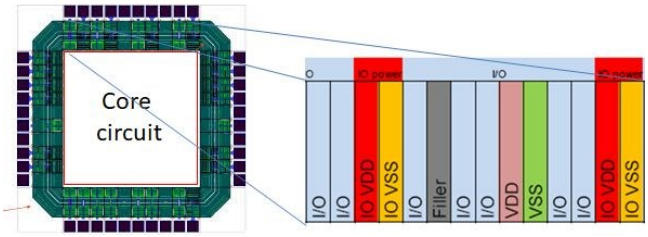

Figure 4: Typical I/O-ring and I/O segment showing different I/O pads side-by-side.

Interfaces that are connected to the outside of the package are frequently designed into an I/O-ring at the edge of the chip. Foundries provide a set of power/ground pads, digital and analog I/O's, corner and filler cells. IC designers can easily create a custom I/O-ring by combining these different

pad-types. Of course, the foundry also provides ESD guidelines on the repetition rate for power pads, minimum number of power pads and the maximum distance for any I/O to a power/ground pad.

On the other hand, interfaces that stay inside the package do not really need a complete I/O ring. A small I/O section close to the Through-Silicon Via (TSV) or pad/bump area can suffice. It is somewhat similar to I/O sections for ball grid area layouts. Of course, it is possible to reuse GPIO cells for such an IO section. As discussed above the I/O options are not always matching the requirements: ESD robustness, the I/O voltage and drive current can all be reduced.

This means that there is a great opportunity to reduce silicon area. It is therefore recommended to use custom I/O and ESD cells. These can be smaller and can be designed with a different aspect ratio. It is also recommended to rely on local I/O protection clamps to reduce the need for nearby power protection clamps.

III. D Summary

ESD protection for 2.5D and 3D packages is different than for regular, single-die packages. IC designers will need customized I/O and ESD solutions because the ESD robustness can be reduced, the signal voltage is outside the standard I/O voltage range, sensitive devices are connected and there is plenty of opportunity to reduce total ESD area.

- A lower ESD robustness can be used. ESD clamps can be scaled down in size
- Local I/O protection can rely on SCR devices with high intrinsic robustness
- If local I/O ESD protection clamps are used there is less need for a nearby power clamp. In some cases the power clamp is not required at all and thus there is also no need to route metal connections to the die-2-die interface area
- Local I/O ESD protection devices can be designed such that the ESD devices can handle different stress combinations. This reduces the number of ESD devices.

IV. ESD protection approach

It is clear that the traditional ESD approach for analog I/O pads, shown in Figure 5 [2-6], is not optimised for die-2-die interfaces.

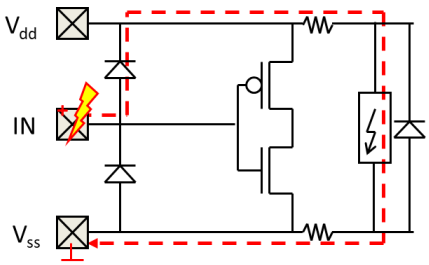

Figure 5: The traditional ESD approach for many I/O pads: A diode from Vss to I/O and another diode from I/O to Vdd. A power clamp is required for half of the stress combinations.

There are several issues with this simple approach, specifically for high speed die-2-die interfaces:

(1) The ESD diodes may introduce excessive parasitic capacitance between the signal pad and the power lines.
(2) Some interfaces cannot tolerate a diode from I/O pad to Vdd due to matching, due to noise coupling between pad and Vdd or because the signal voltage can be higher than the reference Vdd voltage.
(3) For sensitive nodes (e.g. thin oxide gate) the total voltage drop over the intended ESD current path is beyond the failure voltage of the functional circuit.
(4) There has to be a low resistive Vdd connection to the power clamp.

Further in this paper there are examples of optimized ESD protection for die-2-die interfaces. In those projects IC designers replaced the traditional dual diode ESD approach with a local protection clamp concept, simplified in Figure 6. [7-12]. Figure 6 shows a semi-local ESD protection clamp. In some cases a full-local approach (see further in the cases) is used if the circuit between Vdd and I/O is also very sensitive for ESD stress.

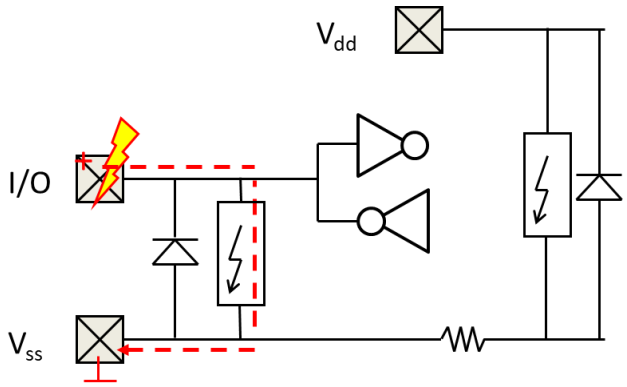

Figure 6: Simplified circuit schematic with a local clamp ESD protection approach.

The local clamp approach introduces a lot of benefits:

(1) Reduced dependence on bus resistance
(2) Strongly reduced voltage drop under ESD conditions without the need for an isolation resistance, perfect for sensitive nodes.
(3) Different options to reduce the parasitic capacitance (see case studies below)
(4) This approach can be optimized for each I/O pad separately, independent from the power clamp strategy.
(5) There is no need for a low resistive connection to the Vdd power clamp
(6) It can also be used for fail-safe, overvoltage tolerant I/Os

V. Co-packaged case studies

Sofics has delivered customized ESD protection for die-2-die interfaces to more than 20 companies for the protection of high-speed SerDes interfaces in 28nm CMOS, 16nm/12nm, 7nm and 5nm FinFET technology. In this paper we present data based on dedicated ESD test chips and product integrations. The paper includes 12nm, 7nm and 5nm examples. The presentation will include additional data from our test chip on Samsung 4nm FinFET.

V.I SerDes protection on 12nm FinFET

Our customer developed a 64 Gbps SerDes circuit and required optimized ESD protection. The SerDes circuit is operated at 0.8V, below the minimum I/O voltage of 1.8V.

Moreover, the parasitic capacitance must be reduced compared to the conventional analog I/O cell. The maximum tolerated capacitance was 100fF. Thus, a custom analog I/O cell design is required.

The functional circuit is designed using thin oxide transistors for the highest interface speed. Such thin oxide transistors are easily damaged during ESD stress. A low trigger and clamping voltage is required to protect the circuit. If it is not possible to place the rail clamp nearby a full-local clamp approach is the best option.

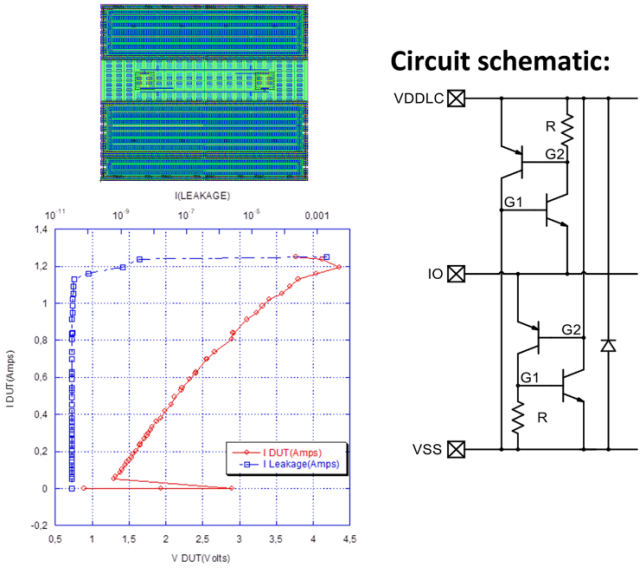

Figure 7: Layout, Simplified circuit schematic and 100ns TLP result (pad to VSS) for the local clamp ESD protection approach.

An initial version of the SCR based local protection was included on a Sofics ESD test chip with the following aspects: Figure 7

- Silicon area: 20.7 um x 17.6 um (<370 um²)
- Total parasitic capacitance less than 65fF
- 50pA leakage current at 0.8V at 25°C
- 1nA leakage current at 0.8V at 125°C
- About 1.5kV HBM protection

Our customer asked for a customized version with another aspect ratio. The layout was changed for their MPW run. The narrow layout increased the parasitic capacitance from the metal connections.

Two ESD protection approaches are compared

- Dual diode at I/O + 0.8V rail clamp
- A full-local ESD clamp concept + 0.8V rail clamp

Both protection approaches have been tested on silicon test chip together with the 64 Gbps SerDes circuit. The main parameters in the comparison are effective protection during CDM stress, parasitic capacitance and silicon area. The target CDM peak current is defined at 6 ampere.

The results of the analysis are shown in Table 1. In this comparison, the dual diode concept is smaller and has lower parasitic capacitance. However, it is less effective in protecting the thin oxide transistors during CDM stress.

Parameter	Dual diode and rail clamp	Local clamp initial layout	Local clamp customized layout
Silicon area [um²]	15.3 x 15.3 < 235 um²	20.7 x 17.6 < 370 um²	10 x 34.3 < 345 um²
Capacitance	71.1 fF	65 fF	91.2 fF
TLP		1.15 A	
HBM		1.5kV	
CDM	600 V		1300 V
CDM current	~5 A		~ 12 A

Table 1: Comparison of the 3 ESD solutions for the protection of 12nm SerDes circuit. The conventional dual diode + rail clamp is compared to customized SCR based full-local ESD protection concepts. The optimized SCR solution achieves the highest CDM robustness. The low trigger and clamping voltage ensures an effective protection of the sensitive thin oxide transistors.

V.II die-2-die interface on 7nm FinFET

Customized local ESD protection cells for 0.75V interfaces were designed for 3 cases on TSMC 7nm FinFET technology, Figure 8. The blue curve shows the ESD cell for interfaces that connect outside of the package. Those pads require standard 2000V HBM robustness. For Silicon photonics applications 2 ESD protection clamps were prepared with strongly reduced parasitic capacitance. These interfaces remain inside the package. The required ESD robustness was reduced to 400V (green) and 150V HBM (red version).

In 7nm FinFET technology, the failure voltage of core transistors (gate to source and drain to source) is about 3V. Fortunately, in many SerDes applications there is a bit more margin due to other transistors connected in series. Failure voltage of those circuits is around 4-5V depending on the circuit concept.

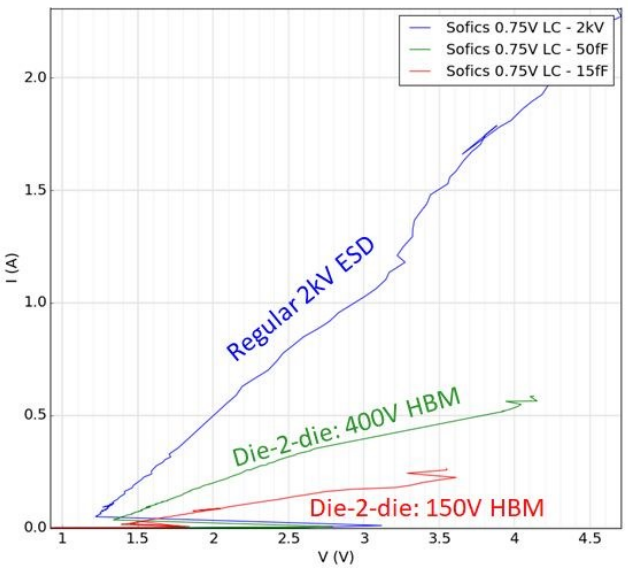

Figure 8: TLP results for Sofics ESD solutions for the protection of interfaces build with thin oxide transistors in 7nm FinFET technology. Three different versions are shown. The blue curve, fit for at least 2kV HBM, can be used for regular interfaces that connect to the outside of the package. The green and red version are a lot smaller and introduce much less parasitic capacitance. These cells have been used to protect die-2-die links in 2.5D Silicon Photonics projects.

Figure 9 shows the layout (left side) and schematic view (right side). A full local ESD protection approach is used to cover all 4 stress cases in the I/O area. There are SCR based clamps between Pad and VSS and between VDD and Pad. There are integrated diodes (in the SCR) between VSS and Pad and Pad and VDD. Finally a separate diode is added between VSS and VDD. Because the 4 stress cases are covered locally the distance to the power clamp is not so important compared to dual diode based ESD protection. The ESD-on-SCR clamp approach requires a current path during triggering. In most cases the leakage from the functional circuits provide ample trigger current. However, if the analog domain is very small, an RC triggered NMOS active clamp between VDD and VSS (small version rail clamp) can be added to reduce the trigger voltage of the ESD-on-SCR devices.

HBM [V]	Capacitance [fF]	Width [um]	Height [um]	Area [um²]	SCR width [um]
150V	15fF	7.43	21.1	<160	2x 3.5
400V	50fF	15.4	21.1	<330	2x 11.5
2kV	Not optimized	24.3	30	<750	4x 20.8

Table 2: Comparison of the different versions on the 7nm FinFET technology.

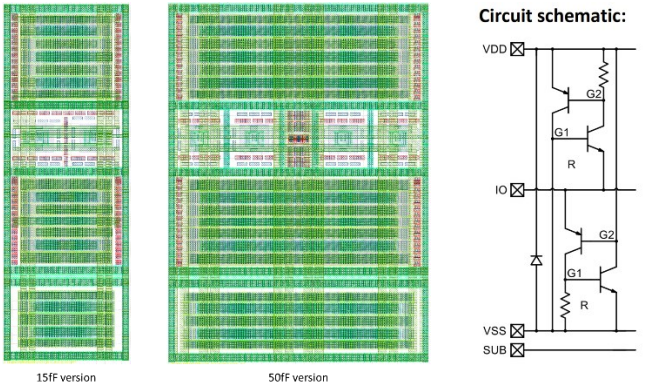

Figure 9: Layout (left) for the 15fF and 50fF clamp versions and the circuit schematic of the full local ESD protection clamp cell (right).

The local ESD protection clamps are built using Silicon Controlled Rectifiers that reach high ESD robustness for a small junction area. This small junction area also leads to low leakage and low parasitic capacitance. The 2kV version is 750um², the other versions are 330um² (400V HBM) and 160um² (150V HBM) respectively (Table 2).

Thanks to the local clamp approach the Vdd-Vss power clamp does not need to be close to the signal pad. The ESD related area at TSV bumps is limited. Moreover there is no need to route a wide Vdd metal connection.

The 7nm low-capacitance ESD clamps have been integrated into designs for high speed interfaces in Silicon Photonics data center applications. The simulated parasitic capacitance over IO voltage for the 15fF version is shown below (Figure 10) for the Typical, Fast and Slow corners. It includes both the junction capacitance (from the Spice model) and Metallization capacitance (based on PEX extraction).

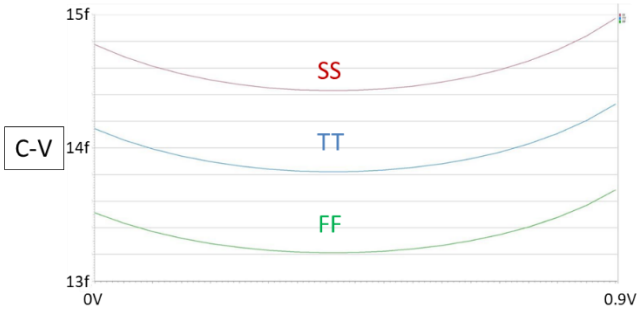

Figure 10: Simulation of the parasitic capacitance of the 15fF version on 7nm, across applied IO voltage and for 3 corners.

To increase the bandwidth, designers integrate many die-2-die interfaces on a single chip. Therefore it is important that the leakage of the single ESD protection device is as low as possible. The analysis on Figure 11 shows that the leakage stays below 1nA in the entire voltage range, even at a higher temperature (125°C).

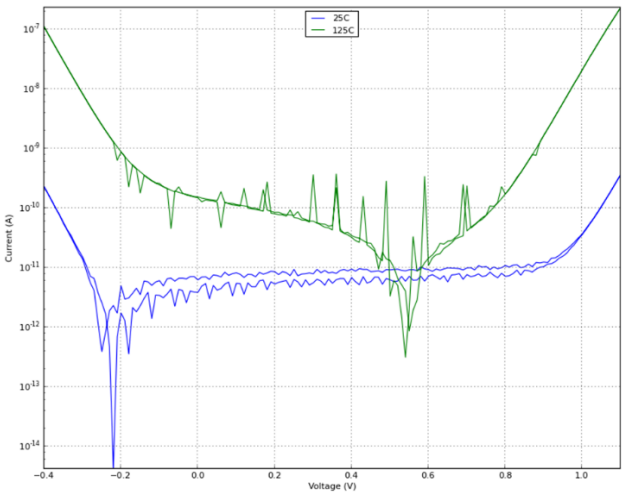

Figure 11: leakage analysis at both 25°C and 125°C for the 7nm FinFET ESD solution designed for 15fF parasitic capacitance (target 150V HBM protection). Even at high temperature the leakage of the ESD protection device remains below 1nA within the entire voltage range (0 to 0.75V).

While the chip assembly house referred to minimum HBM values (150V) for the die-2-die connections the main challenge for circuits based on thin oxide transistors is CDM stress. To verify the effectiveness of the protection circuit, VF-TLP measurements were performed using 5ns pulse width and 200ps fast rise rime. The pulses are delivered through a 50 Ohm transmission line and high-frequency wafer probes to the 7nm bare die samples. The VF-TLP result is shown in Figure 12, below. More than 5 ampere was reached.

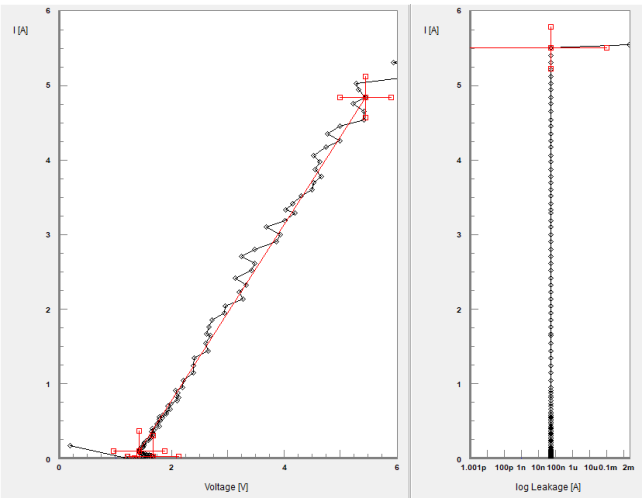

Figure 12: VF-TLP analysis of the SCR local clamp concept on TSMC N7 technology, suitable for interfaces based on core devices. The VF-TLP used 5ns pulses and 200ps rise time.

V.III Die-2-die interface on 5nm FinFET

Several customers asked for ESD protection solutions with low parasitic capacitance on the most advanced FinFET node. Different ESD concepts have been added on a dedicated test chip on N5 technology. An initial measurement for a local clamp suitable for protection of interfaces based on core devices is shown in Figure 13. The device is measured on our first 5nm test chip. It was not optimized yet for a specific ESD robustness. This cell reaches about 1.5kV HBM. For the die-2-die interface the ESD robustness can be further reduced.

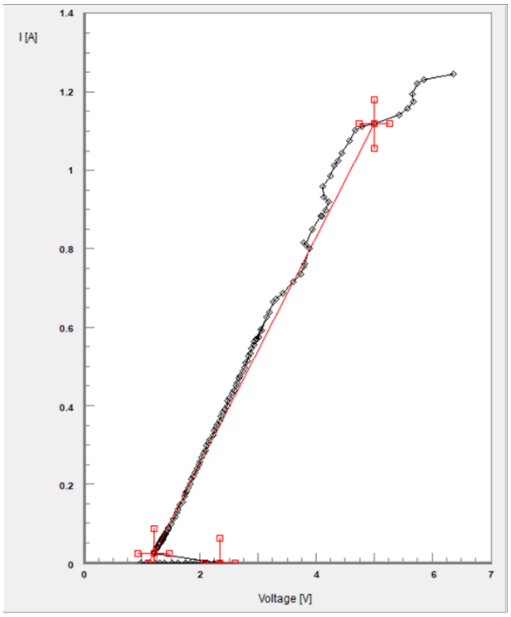

Figure 13: Initial TLP analysis of the SCR local clamp concept on TSMC N5 technology, suitable for interfaces based on core devices.

For a high-speed interface design (112Gbps SerDes Tx) the local clamp ESD protection was customized to reduce the parasitic capacitance. This customization mostly involves changing the aspect ratio and adapting the metal connections to reduce parasitic capacitance from the metal lines. After a study of the functional circuit the ESD design windows were determined for the 4 stress cases that involve the IO pad. It was decided to employ a full-local ESD protection similar to the 12nm and 7nm cases (Figure 7and Figure 9).

The new ESD clamp (Figure 14) is designed to provide 1kV HBM robustness. The optimized clamp is then used by our customer to protect 1.0V IO – SerDes Tx circuits in TSMC 5nm FinFET technology based on core transistors.

The parasitic capacitance of the junctions and metal connected to the IO-pad is about 90fF based on simulations with the foundry provided diode models and parasitic extraction of the metal connection. The clamp leakage is well below 1nA at 1.2V bias.

The combination of the SerDes circuit and ESD protection cell was measured on a 5nm test chip. Thanks to the ESD-on-SCR concept, the trigger voltage and clamping voltage remain very low at about 1.3V. The clamping voltage at 1kV HBM is about 3.7V. The clamp failed at 1.9kV HBM.

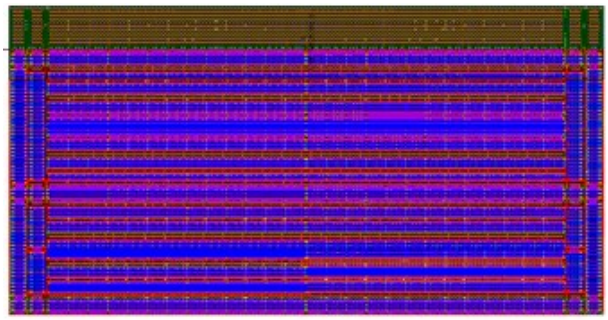

Figure 14: Layout plot of the local IO ESD clamp in TSMC 5nm technology. Total area is less than 250um² (11.384um x 21.952um). The area includes 2 SCR devices, similar to the full-local protection concepts used in the 12nm and 7nm case.

CDM was measured in a large package. The combination of the functional SerDes circuit and the ESD protection device reached 300V CDM, for a peak current of more than 6.5A.

Discussion

Because the die-2-die interfaces remain inside the package it is not really relevant to define HBM or CDM robustness levels. The robustness level cannot be measured in a final product because the internal/hidden pins cannot be touched. However, the interface circuits could be damaged during CDM stress of pins that connect to the outside of the package. It is easy to understand that die-2-die connections can be considered similarly as interdomain interfaces inside a large SoC (system on chip) product. In those interdomain cases, it is important to add (smaller) ESD protection.

In the example cases discussed above, the holding voltage (1.2V – 1.5V) is high enough because the functional operation signals that are lower than 1.2V. If the same ESD approach is used for a product with higher signal voltage (1.8V, 2.5 or 3.3V), additional diodes are added to increase the holding voltage. Beyond 3.3V we tend to use other protection concepts with an intrinsic higher clamping voltage.

Conclusions

ESD protection for 2.5D and 3D packages is different than for regular, single-die packages. IC designers need customized I/O and ESD solutions because the ESD robustness can be reduced, the signal voltage is outside the standard I/O voltage range, sensitive devices are connected and there is plenty of opportunity to reduce total ESD area.

The traditional ‘dual diode’ ESD protection concept for analog I/O pads creates too much voltage drop during ESD stress leading to failure of core transistors connected to die-2-die interfaces. This work showed case studies where the dual diode concept was replaced with local ESD protection clamps in the I/O pad based on proprietary SCR devices. The local clamp reduces the dependence of the bus resistance, reduces the clamping voltage and allows to optimize every analog I/O separately. Moreover, the cases show that it is possible to create ESD protection with a very low parasitic capacitance and small silicon footprint.

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