Optimized Local I/O ESD Protection for SerDes In Advanced SOI, BiCMOS and FinFET Technology

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Abstract - Semiconductor companies are developing ever faster interfaces to satisfy the need for higher data throughputs. However, the parasitic capacitance of the traditional ESD solutions limits the signal frequency. This paper demonstrates low-cap Analog I/Os for high speed SerDes (28Gbps to 112Gbps) circuits created in advanced BiCMOS, SOI and FinFET nodes.

I. Introduction

In the connected world today, the demand to transfer data is growing every day. People increasingly consume streaming video content, at home and on the road. The increased bandwidth is needed on every level, from smartphones, PCs, at data centers and across long distance connections. This demand pushes the semiconductor industry to develop faster communication solutions for wireless, optical and wired interfaces. A few years ago, the speed limit was in the order of 10 Gbps. Recent circuits run at 56Gbps or even 112Gbps.

For such high-speed communication interfaces chip designers need to limit the parasitic capacitance of the on-chip ESD protection clamps connected to the interfaces. Because the traditional ESD approach is not good enough, they need special analog I/O circuits. This paper demonstrates silicon proven ESD solutions on advanced SiGe BiCMOS, 22nm FD-SOI and 16nm and 7nm FinFET technology. Parasitic capacitance of the ESD solutions is reduced below 100fF and for some silicon photonics applications even below 20fF.

II. Traditional ESD approach

The traditional ESD approach for analog I/O pads is shown in Figure 1. It consists of a diode from Vss to the I/O pad, a second diode from I/O pad to Vdd and a power/rail clamp between Vdd and Vss [1-5].

IC designers like it because the 2 diodes are easy to implement, have a small silicon footprint and have reasonably low parasitic capacitance.

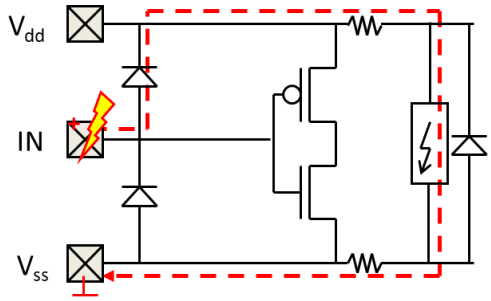

Figure 1: The traditional ESD approach for many I/O pads: A diode from Vss to I/O and another diode from I/O to Vdd. A power clamp is required for half of the stress combinations.

For sensitive nodes, IC designers add an isolation resistance from I/O to the circuit to increase the ESD design window. If the functional circuit cannot handle any ESD current, a secondary clamp is added behind the isolation resistance (Figure 2).

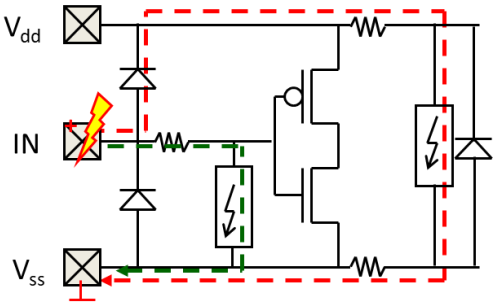

Figure 2: Sometimes IC designers add a resistance between I/O pad and the circuit and implement a small secondary clamp just before the sensitive circuit. This increases the ESD design window.

There are several issues with this simple approach, specifically for high speed interfaces:

(1) The isolation resistance severely impacts behaviour at high speeds and adds noise.
(2) The ESD diodes may introduce excessive parasitic capacitance between the signal pad and the power lines.
(3) Some interfaces cannot tolerate a diode from I/O pad to Vdd due to matching, due to noise coupling between pad and Vdd or because the signal voltage can be higher than the reference Vdd voltage.
(4) For sensitive nodes the total voltage drop over the intended ESD current path can be above the failure voltage of the functional circuit [5].

A simple way to reduce the capacitance (issue 2) and increase the voltage tolerance (issue 3) is to use 2 or more diodes in series. However, this leads to a higher voltage drop during ESD stress, deteriorating issue 4. An alternative with a novel dual bipolar concept was presented in 2017 [6-7].

This paper discusses projects where IC designers replaced the traditional dual diode ESD approach with a local protection clamp concept, simplified in Figure 3. If the functional operation cannot tolerate a diode from 'IN' to Vdd that diode can be removed. That is typical for fail-safe, hot-swap, open-drain outputs, cold-spare inputs or overvoltage tolerant interfaces [8].

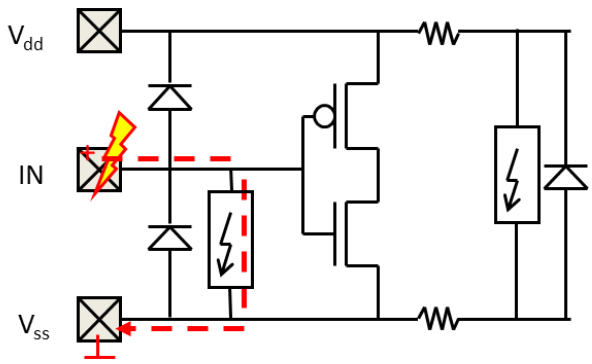

Figure 3: Simplified circuit schematic with a local clamp ESD protection approach. The diode between IN and Vdd can be removed if needed for the functional operation. In some cases, another clamp is added between Vdd and 'IN'.

The local clamp approach introduces a lot of benefits:

(1) Reduced dependence on bus resistance
(2) Strongly reduced voltage drop under ESD conditions without the need for an isolation resistance, perfect for sensitive nodes.
(3) Different options to reduce the parasitic capacitance (see case studies below)
(4) Can be optimized for each I/O pad separately. E.g. some pads may need higher ESD robustness or cannot tolerate a diode between I/O and Vdd.

The next part of the paper includes several case studies where a local clamp approach was used to protect high speed interfaces demonstrating low parasitic capacitance, low leakage and within a small silicon footprint.

III. SCR based local I/O clamp

Different types of SCR-based local clamps are used in the case studies (Figure 4). The Diode triggered SCR and ESD-on-SCR were previously used to protect wireless LNA interfaces [9].

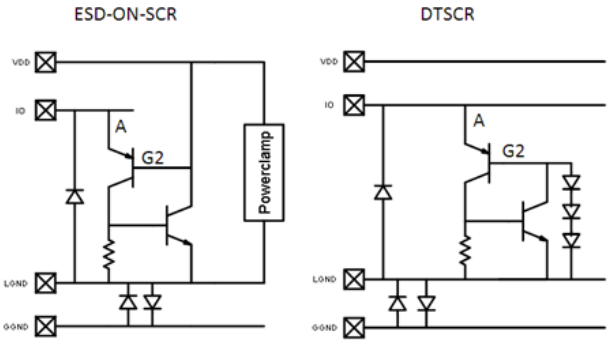

Figure 4: Two ESD protection clamps used in the case studies. The Sofics ESD-on-SCR is triggered as soon as the IO level raises 1 diode drop (Anode-G2) above the Vdd voltage. The Sofics DTSCR is turned on once the AnodeG2 and trigger diodes are forward biased.

A. ESD-on-SCR

The ESD-on-SCR (Figure 4, left side) is a simple concept. The Nwell (G2) is tied to Vdd. The anode is connected to the I/O pad. Cathode (N+) and G1 terminals are connected to ground. During normal operation the Vdd potential is higher than or equal to the I/O voltage. The Anode-G2 junction remains reverse biased. The SCR is in a high-impedance

state. Because there is no trigger device the leakage of the clamp (I/O to Vss) is also very low.

During ESD stress from I/O to ground the Vdd supply line is floating. Initial ESD current flows through the Anode-G2 junction into the floating Vdd bus and the circuits between Vdd and Vss. This initial part is actually similar to a dual diode based I/O protection. Current flowing through the Nwell diode from pad to Vdd will cause a rapid rise of the Vdd potential. It could lead to a turn on of the Vdd-Vss railclamp. In the dual-diode case the ESD current will flow through the diode, the Vdd bus to the power clamp and then the rail clamp to ground. As explained in part II, this traditional approach may cause a failure of the functional circuits if the total voltage drop of this ESD current path is excessive.

The parasitic PNP inside the Nwell diode will also inject current in the substrate (Collector – emitter current) as a function of the base current (SCR Anode – G2) flowing into the Vdd line. In a dual diode concept the current injected into the substrate is picked up by the substrate ties/ring close to the diode. In the case of the ESD-on-SCR the current lifts up the base of the parasitic NPN transistor. This will eventually forward bias the G1-Cathode junction, turning on the NPN transistor. This is the start of a positive feedback loop between the PNP and NPN transistors which leads to a low clamping voltage (~1.2V) between I/O and Vss, protecting sensitive circuits.

B. Diode triggered SCR (DTSCR)

The Diode triggered SCR (Figure 4, right side) is different. In this case there is no diode from I/O pad to Vdd. During functional operation, at signal voltage of about 1.2V or lower the DTSCR device is in a high impedance state.

During ESD stress, ESD current first flows through the chain of diodes between I/O pad and ground. On the example of Figure 4 there are 3 diodes between the G2 node and Vss. The Anode-G2 junction is a 4th diode in the chain. At about 3V at the I/O pad, these 4 diodes are forward biased. Similarly to the ESD-on-SCR device, base current (Anode-G2) in the PNP transistor leads to collector-emitter current from Anode to the local substrate. This current lifts up the base of the parasitic NPN device, turning it on as well. The positive feedback is started and the SCR shunts ESD current from Anode to Cathode during a low impedance state at about 1.2V.

In both cases it is important to consider the layout of the SCR structure. The further apart the Anode and Cathode, the longer it takes for the positive feedback to kick in. The longer it takes for both NPN and PNP devices to work in tandem, the higher the voltage will rise. This is especially important during fast events like CDM ESD stress. In the last chapter, further down, VF-TLP measurements are used to quantify the turn-on time of the SCR devices.

IV. SerDes protection case studies

Several local clamp approaches with (ultra) low parasitic capacitance are summarized in case studies below for the protection of high-speed SerDes interfaces in 28nm CMOS to 5nm FinFET.

A. FPGA 28nm, 28Gbps SerDes

For a range of advanced FPGA products in TSMC 28nm the designers requested custom ESD protection cells. For the 28Gbps SerDes interface the following specifications were required.

- Parasitic capacitance well below 100fF.
- ESD rating: > 1kV HBM; >250V CDM

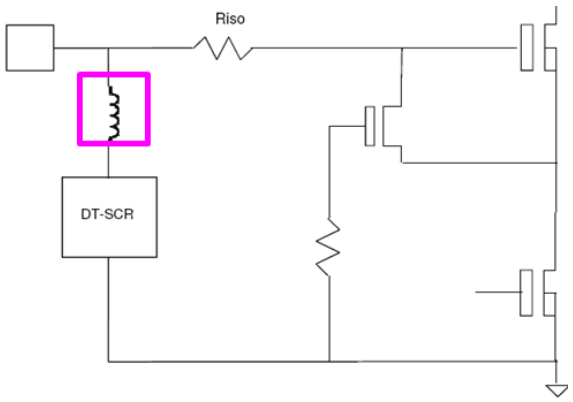

Figure 5: Schematic representation of the 28Gbps SerDes Rx (input) stage, showing the DTSCR local clamp and secondary protection stage for enhanced CDM protection.

A scaled-down version of the Sofics DTSCR clamp was selected as the local protection for the Tx and Rx interfaces. A secondary local CDM clamp was added behind the isolation resistance to protect the thin oxide gate oxide in the Rx case (Figure 5). The parasitic capacitance of the DTSCR, the reverse diode and the metal connections together was reduced below 80fF.

In order to meet the S11 – Return loss specification an inductor was added in series with the DTSCR (Figure 6). All specifications were met including CDM. The part reached more than 300V with a 4.5A peak current [10].

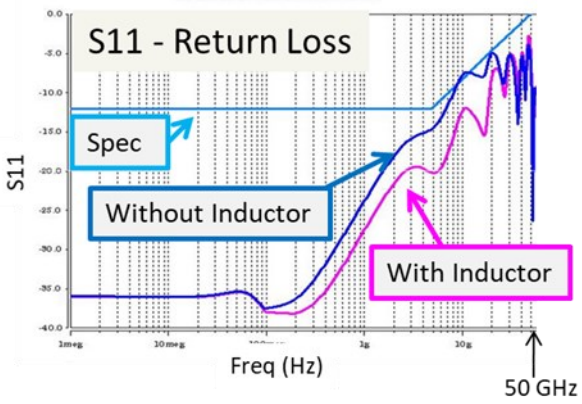

Figure 6: To meet the S11 specification an inductor was added in series with the DTSCR. The coil reduces the S11 peaks at 10 GHz and 20 GHz.

B. Generic SerDes 16nm, 28Gbps

A high speed (data center) communication chip with a 28 Gbps SerDes, produced in 16nm FinFET technology required a custom ESD protection approach.

The local ESD clamp must adhere to these requirements.

- Protection of sensitive thin oxide, 0.8V core transistors with failure voltage during ESD stress below 3.3V
- Low leakage ESD clamp, below 10nA at high temperature (125°C)
- Small silicon footprint to enable multiple channels on the same communication chip
- No resistance allowed
- >2kV HBM
- Maximum ESD junction capacitance of 100fF.

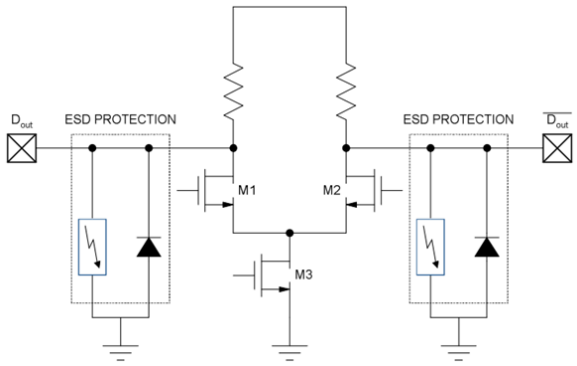

Figure 7: Schematic representation of the protection concept for the differential pair of the Tx interface. On both paths of the differential pair a local clamp and parallel reverse diode is added.

Based on an extensive test chip analysis on TSMC 16nm FinFET technology the ESD-on-SCR concept was selected as the local clamp device.

The TLP data is shown on Figure 8. In an area of less than 1.000 um² (less than one thousand um²), it protects thin-oxide devices above 2 Ampere. Leakage at high temperature is about 1nA.

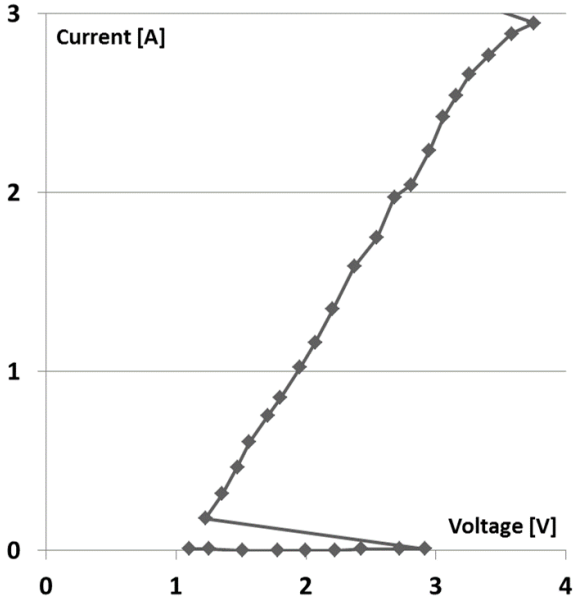

Figure 8: TLP measurement of the ESD-on-SCR device used as local clamp device. The device reaches more than 2A before the failure voltage of thin oxide transistor is reached.

To ensure that the ESD protection clamp does not influence the functional operation of the high speed SerDes, the parasitic junction capacitance is

simulated across pad voltage, shown in Figure 9. An equivalent model based on diode junctions was used to simulate the capacitive loading of the ESD cell.

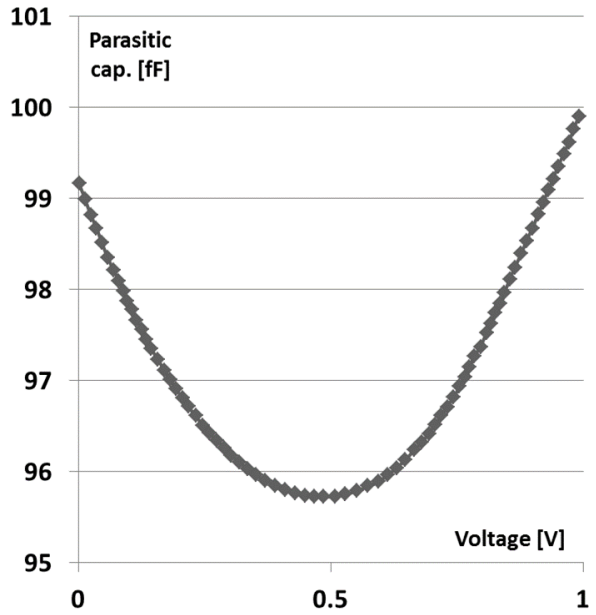

Figure 9: Capacitance simulation (Spice) for the ESD-on-SCR. The capacitance remains below the target level of 100fF across the entire voltage range of the pad

C. Silicon Photonics 28nm, 28Gbps

Several companies working on new optical transceivers contacted us for support. For the regular, low speed I/Os (1.8V) the Analog/digital I/O library provided by the foundry was sufficient. The ESD requirement for those pads was 2kV HBM.

On the other hand, the analog I/Os in the foundry library introduced too much parasitic capacitance for the high-speed interfaces. The designers requested a reduced total capacitance of the ESD device below 15fF.

The 28nm CMOS SoC was co-packaged with a silicon photonic device in a shared/hybrid integrated package (Similar to Figure 10). Because this flip-chip assembly is performed in an ESD controlled environment the ESD protection level could be reduced to 200V HBM without effect on the yield.

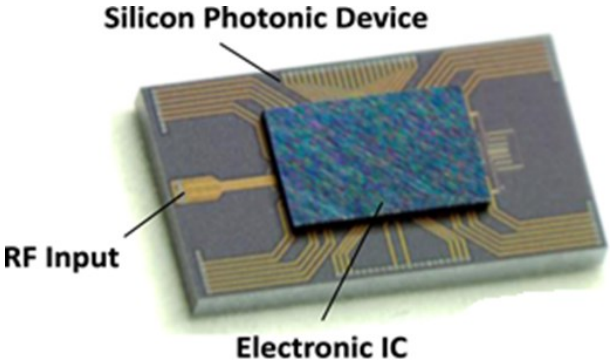

Figure 10: (Example) Packaging of an electronic IC (driver) on a silicon photonic device using a flip-chip bonding process (© IOP 2016 [11])

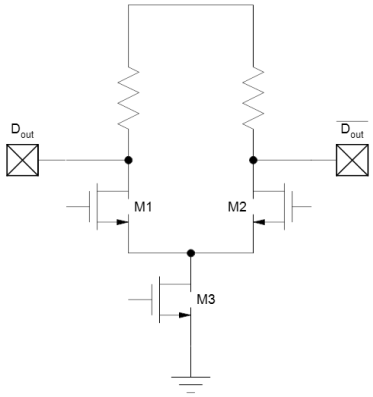

Figure 11: Simplified Tx/output circuit used in the Silicon Photonics SerDes interface.

The 28Gbps interfaces used a differential pair concept as shown in Figure 11. The 1V functional circuit is created using 0.9V core transistors to ensure the switching speed can be reached. However, these transistors reduced the available ESD design window for the Rx, Tx signals to 4V.

Other requirements for the ESD protection included low leakage operation and small silicon footprint.

The ESD protection design consists of a full local protection clamp concept, shown in Figure 12. A 1V power clamp was integrated to ensure all the stress cases could be handled locally at the interface and bus resistance is taken out of the equation. The entire clamp structure was isolated from the substrate to reduce noise from the substrate that could come from digital circuits further on the die.

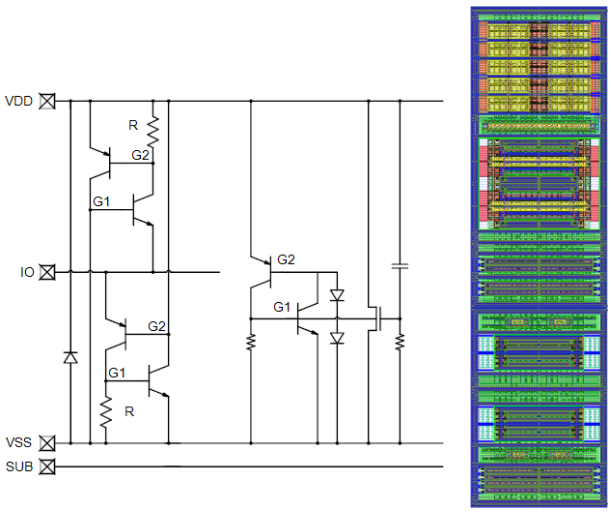

Figure 12: Schematic view (left) of the full local protection approach for the Rx and Tx nodes of the SerDes circuit. It is based on ESD-on-SCR devices. An SCR based 1V power clamp is integrated in the same layout (right). The total area for ESD is 683.75 um².

The total parasitic capacitance at the I/O pad consists of different aspects. The junction capacitance can be easily derived from the foundry provided Spice models for diodes. The metal connections to the local ESD clamps can add a significant amount of capacitance. The parasitic metal capacitance can be derived from PEX extraction. Reducing the width of the metal connections can reduce the capacitance but will also reduce the robustness of the connection. The minimal metal width is derived from ESD stress performed at different metal stripes on our ESD test chip. Metal dummies (requirement for CMP in advanced processes) are included in the PEX extraction when customers request ESD protection with ultra-low capacitance (well below 100fF).

Through an iterative process (layout, PEX extraction) the total parasitic capacitance of the ESD clamp was reduced to less than 15fF. The presentation will show the different steps in this procedure. The plot below (Figure 13) shows the capacitance value as function of the bias voltage at the pad.

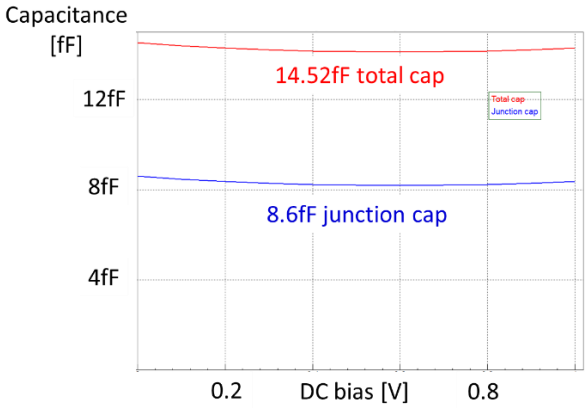

Figure 13: Parasitic capacitance (total and junction only) across the I/O voltage for the full local ESD protection clamp designed in a TSMC 28nm technology.

The parasitic capacitance to ground must be reduced to prevent that the high-frequency signal is shunted to ground.

$$X_C = \frac{1}{\omega C} = \frac{1}{2\pi f C}$$

Equation 1: The capacitor reactance Xc (in Ohm) inversely proportional to the signal frequency (f) and capacitance (C)

For high frequency (>50 Ghz), the parasitic capacitance behaves as a resistance to ground. This impedance must be high enough. A 15 fF capacitance behaves as a ~200 ohm resistance at 50 GHz.

In the iterative process to reduce the contribution of the parasitic capacitance from the metal connections a number of rules are used

- Remove unnecessary via connections
- Reduce Metal 1 as much as possible, keep it on top of the connected diffusion only.
- Prevent running Metal 1 across junctions.
- Work vertically (up) for connections

Even when reduced, more than 40% of parasitic ESD capacitance can be linked to the metal connections in advanced nodes.

Using a transient Spice simulation of HBM ESD stress, the local clamp approach of Figure 12 is compared with 2 other concepts.

- Concept 1: Proposed local clamp
- Concept 2: Foundry provided I/O pads (dual diode and foundry proposed core power clamp)
- Concept 3: Dual diode combined with Sofics 1V core protection clamp

From Figure 14 it is clear that concept 2 and 3 create a voltage drop well above the failure voltage (4V) of the sensitive circuit based on thin oxide transistors [12].

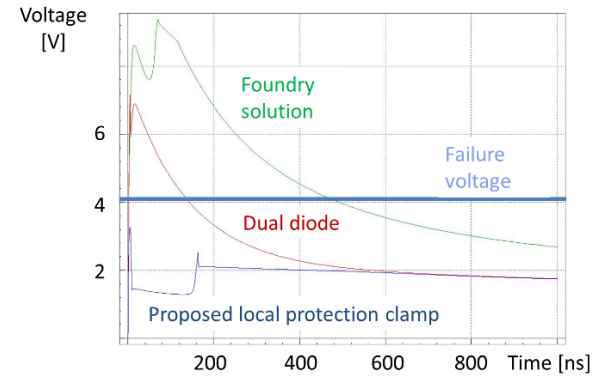

Figure 14: Transient Spice simulation under HBM stress. 3 concepts are compared to verify that the voltage drop at the sensitive node during ESD stress remains below the maximum level of 4V. Only the proposed local clamp can shunt the ESD stress below 4V. This comparison was done using 1kV HBM stress with ESD devices scaled to 1kV robustness. The snapback of the SCR local clamp was simulated using a combined NPN/PNP model.

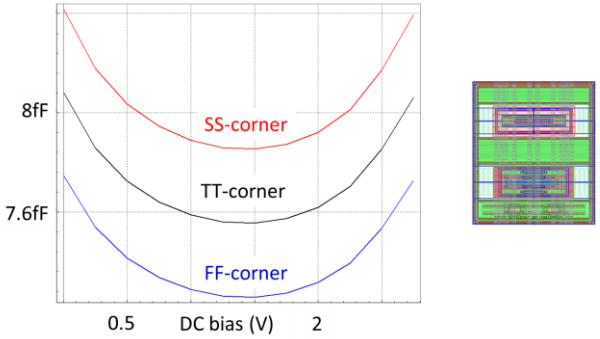

Figure 15: Total parasitic capacitance (junction and metal contributions) across the I/O voltage for 3 corners. The clamp layout is shown on the right side. The full local protection for 100V HBM fits within 217um² and features a leakage of less than 10nA at 125°C.

Another customer asked for a similar ESD solution, but with further reduced parasitic capacitance to ensure an even higher bandwidth. Their assembly provider could ensure enough yield in the hybrid integration (as shown in Figure 10) if the interfaces are robust up to 100V HBM. The simulated parasitic capacitance (junction + metal contributions) for the local protection clamp are shown in Figure 15.

D. Silicon Photonics using a SiGe BiCMOS process

The 90nm BiCMOS chip is co-packaged with a silicon photonic device in a shared/hybrid integrated package and SiPho module. Because this flip-chip assembly is performed in an ESD controlled environment the ESD protection level could be reduced to 200V HBM without effect on the yield.

The 2.5V high-speed interfaces (Tx/Rx) are built with bipolar devices that are sensitive to ESD stress. Other requirements for the ESD protection included low leakage operation and small silicon footprint.

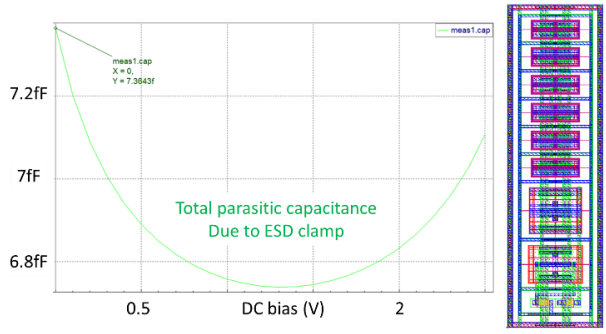

Figure 16: Simulated parasitic capacitance across the I/O voltage. The ESD clamp layout is shown on the right side (11.02um x 37.3um).

The ESD protection clamp in the analog I/O is designed in a footprint of 412um² (Figure 16) and includes a full local protection scheme. A power clamp is integrated to ensure all the stress cases could be handled locally at the interface and bus resistance is taken out of the equation. The leakage is around 10pA at 25°C.

E. Silicon Photonics on 7nm FinFET

To further increase the bandwidth of the optical interconnects (beyond 56 Gbps) our customer moved to TSMC 7nm FinFET technology.

The proposed solution is similar to Figure 12. Two versions of the ESD protection are created, one with parasitic capacitance of 50fF and a smaller version with less than 15fF.

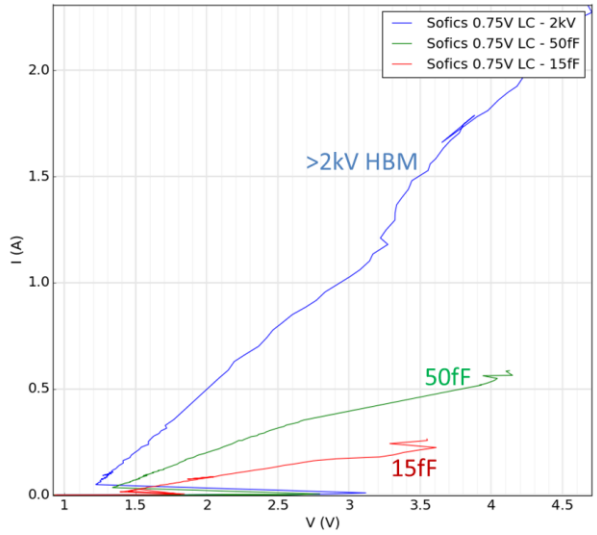

Figure 17: Silicon results on the TSMC N7 process. TLP results for 3 versions (with different target requirements) of the ESD-on-SCR concept. The

Measurements on TSMC's 7nm FinFET process demonstrate that the ESD-on-SCR local clamp performs as expected (Figure 17).

In 7nm technology, the failure voltage of core transistors (gate to source and drain to source) is about 3V. Fortunately, in many SerDes applications there is a bit more margin due to other transistors connected in series (Figure 11). Failure voltage of those circuits is around 4-5V depending on the circuit concept.

The 7nm low-capacitance ESD clamps have been integrated into 2 designs for high speed interfaces. The simulated parasitic capacitance over IO voltage for the 15fF version is shown below (Figure 18) for the Typical, Fast and Slow corners. It includes both the junction capacitance (from the Spice model) and Metallization capacitance (based on PEX extraction).

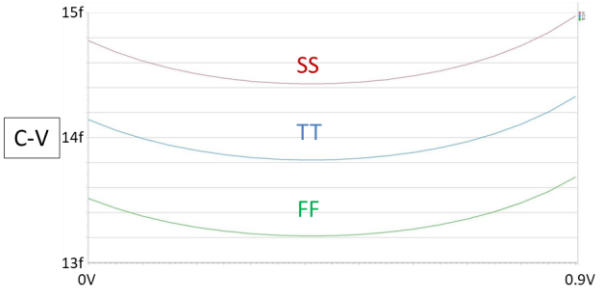

Figure 18: Simulation of the parasitic capacitance of the 15fF version on 7nm, across applied IO voltage and for 3 corners.

Besides low parasitic capacitance, the ESD-on-SCR solution also has a low leakage, orders of magnitude lower compared to the ESD solution proposed by the foundry. The leakage measurement for the 15fF version is shown in Figure 19

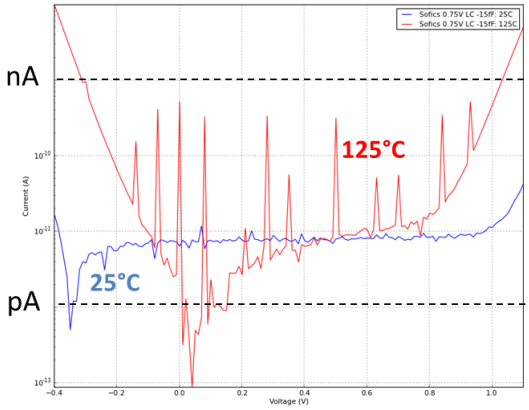

Figure 19: Leakage measurement at low (25°C) temperature and high (125°C) temperature. Even at high temperature, the leakage of the ESD solution remains below 1 nA within the entire voltage range (0 to 0.75V).

F. ESD protection on 22nm FD-SOI

For a number of applications IC designers turn to SOI, to reduce power consumption for instance. GlobalFoundries claims that their 22nm FDX technology is perfect for advanced mm-wave applications. The junction capacitance is indeed reduced thanks to the shallow junctions confined by the buried oxide. The process has a lot of options to optimize the performance and leakage for different parts of the SoC design. There are different MOS Vth variations available. Through the use of the back-gate biasing technique the parameters can even be changed during operation.

On a recent test chip, several ESD protection concepts were verified in this advanced thin-film SOI process. The process supports both hybrid (bulk) and SOI-only design on the same wafer. Diodes and SCRs designed with the BOX removed (hybrid) can achieve higher ESD robustness in the same area. The hybrid SCR version reaches about 24mA/um, a current density comparable to advanced bulk processes. The SOI version fails at 3.5m/um (factor 7 lower) and also has a 4 times higher on-resistance.

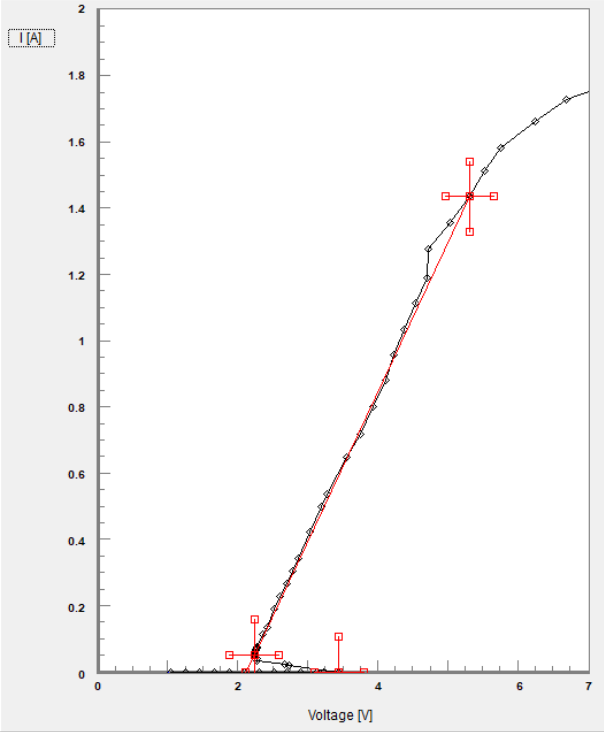

Figure 20: Diode Triggered ESD protection clamp with 2 trigger diodes and 1 holding diode on GF 22nm FDX technology for 1.8V interface protection up to 2kV HBM.

It is clear that ESD diodes and SCR devices should be designed using the hybrid layout style. However, for some parts of the ESD structures the SOI option can be a better option. For instance, trigger diodes of a diode triggered SCR (DTSCR) clamp can be designed in the SOI layout style to prevent leakage increase due to the Darlington effect.

G. ESD protection for N5 FinFET

Several of Sofics customers asked for ESD protection solutions with low parasitic capacitance on the most advanced FinFET node. Different ESD concepts have been added on a dedicated test chip on N5 technology. An initial measurement for a local clamp suitable for protection of interfaces based on core devices is shown in Figure 21.

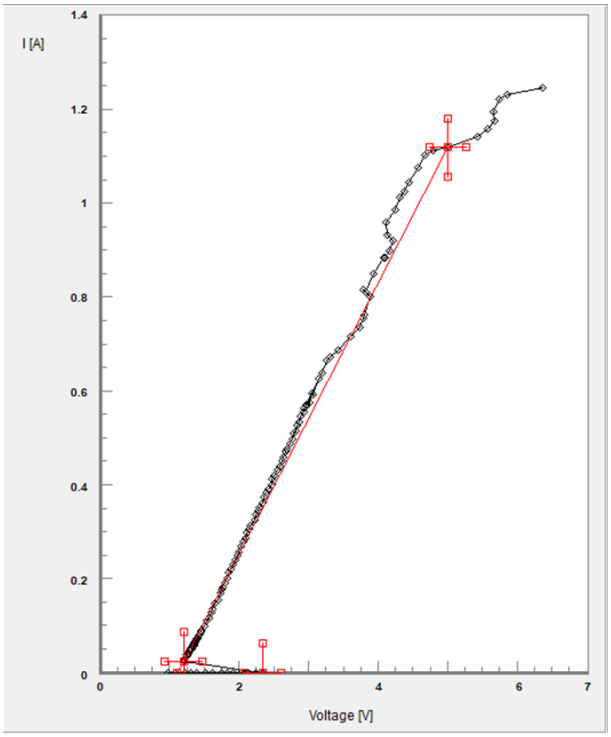

Figure 21: Initial TLP analysis of the SCR local clamp concept on TSMC N5 technology, suitable for interfaces based on core devices.

For a high-speed interface design (112Gbps SerDes) the local clamp ESD protection was customized to reduce the parasitic capacitance. The clamp is designed to provide at least 1kV HBM robustness. The schematic of the local protection is similar to the approach shown in Figure 12. There is an ESD-on-SCR clamp for positive stress from the IO-pad to Vss and another ESD-on-SCR clamp for positive stress from Vdd to the IO-pad. In the 2 other stress directions a diode is integrated in the approach. For ESD stress from Vdd to Vss a separate power clamp is required.

The clamp is used to protect 1.0V IO circuits in TSMC 5nm FinFET technology. The parasitic capacitance of the junctions and metal connected to the IO-pad is about 90fF based on simulations with the foundry provided diode models and parasitic extraction of the metal connection.

The clamp leakage is well below 1nA at 1.2V bias (Figure 22).

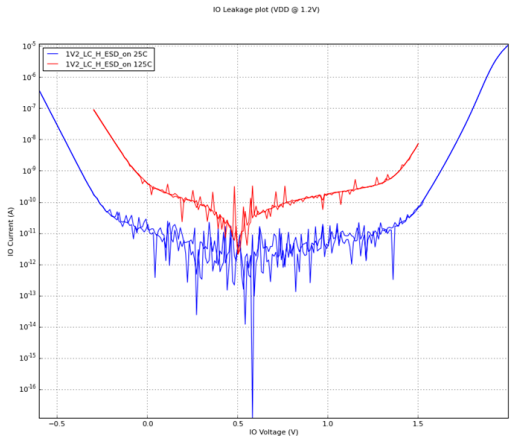

Figure 22: Leakage measurement of the local ESD protection clamp for a 1.0V high-speed interface in TSMC 5nm technology. Data for room temperature and 125°C are shown in the relevant voltage range.

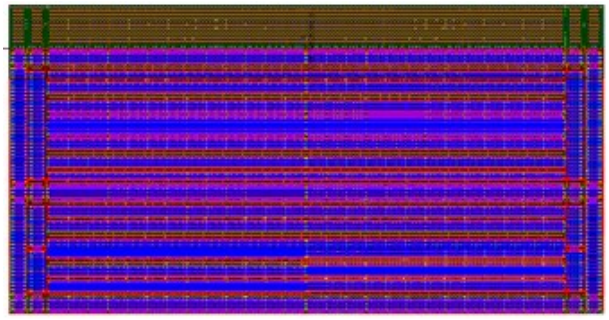

Figure 23: Layout plot of the local IO ESD clamp in TSMC 5nm technology. Total area is less than 250um² (11.384um x 21.952um).

V. CDM protection

For ICs manufactured in advanced nodes, the most relevant ESD test/qualification approach is the Charged Device Model (CDM). The fast-transient stress can rupture thin gate oxides or even damage sensitive drain-source junctions of NMOS devices. Indeed, in the most advanced nodes, core transistors typically fail during snapback, even during short pulses.

Unfortunately, it is not possible to assess CDM protection capabilities (expressed in Volt) based on a test chip. The CDM voltage depends on the product layout, its package size and type. Actual CDM robustness voltage level can thus only be assessed on a complete, packaged product. Sofics does not receive qualification data (HBM, MM, CDM) from its customers when its ESD solutions are integrated into full products.

It is common practice [13, 14] to use a very-fast TLP (VF-TLP) test system with short pulses (e.g. 5ns) and fast rising pulse edges (e.g. 200ps) to quantify the amount of current that can be shunted during fast (CDM) transients. People correlate the ESD current level from such a VF-TLP test to a CDM voltage for different package sizes based on Figure 24.

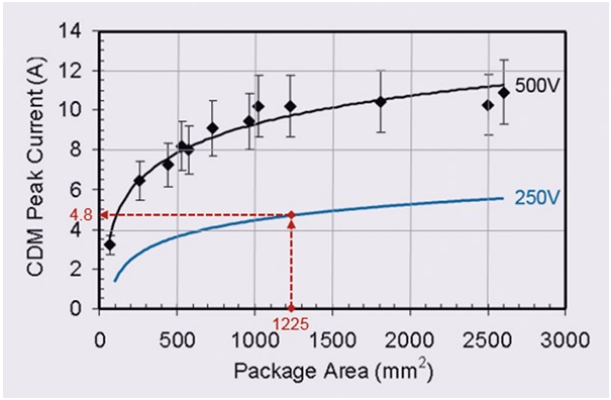

Figure 24: Determination of the target CDM current for a 250V CDM robustness on a 1225um² BGA product [14].

Sofics uses this same technique to ensure the ESD clamps can turn-on fast enough. VF-TLP pulses (width of 5ns, rise time of 200ps) are applied through a50 Ohm transmission line and high-frequency RF probe needles to 2 terminal test structures on bare test chip dies. Example TLP curves are shown below in Figure 25 (16nm FinFET) and Figure 26 (12nm FinFET).

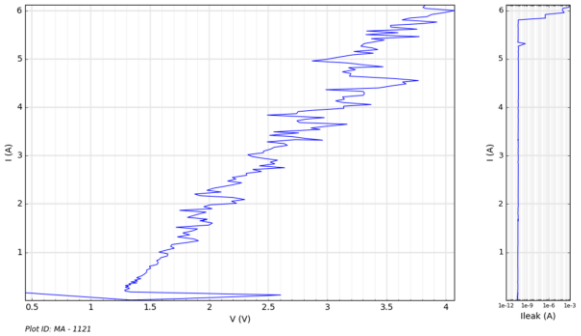

Figure 25: VF-TLP analysis on a 16nm ESD solution, reaching more than 5A.

In the examples related to Silicon Photonics, the CDM level is not relevant because the high-speed interface connections are not accessible outside of the module. At best, the protection needs to be

considered as an interdomain case under CDM stress.

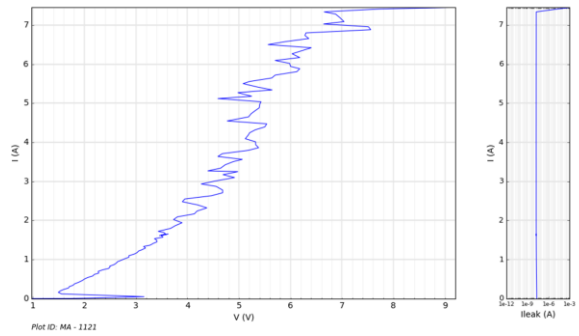

Figure 26: VF-TLP analysis on a 12nm ESD solution (IO to VSS stress), reaching more than 5A.

VI. Conclusions

The traditional 'dual diode' ESD protection concept for analog I/O pads runs into problems for the protection of high speed SerDes interfaces in advanced CMOS and FinFET nodes. The total voltage drop over diode, bus resistance and power clamp easily exceeds the failure voltage of core transistors. Moreover, the 'diode up' adds limitations.

This work showed several case studies where the dual diode concept was replaced with local ESD protection clamps in the I/O pad based on proprietary Diode triggered and ESD-on-SCR devices. The local clamp reduces the dependence of the bus resistance, reduces the clamping voltage and allows to optimize every analog I/O separately. Moreover, the cases show that it is possible to create ESD protection with a very low parasitic capacitance and small silicon footprint.

The data is based on dedicated ESD test chips on advanced CMOS, SOI and FinFET nodes. The analog I/Os in this work are used by more than 20 companies for the protection of high-speed SerDes interfaces in 28nm CMOS, 16nm/12nm, 7nm and 5nm FinFET technology.

VII. Acknowledgements

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