ESD protection for 2.5D and 3D packages

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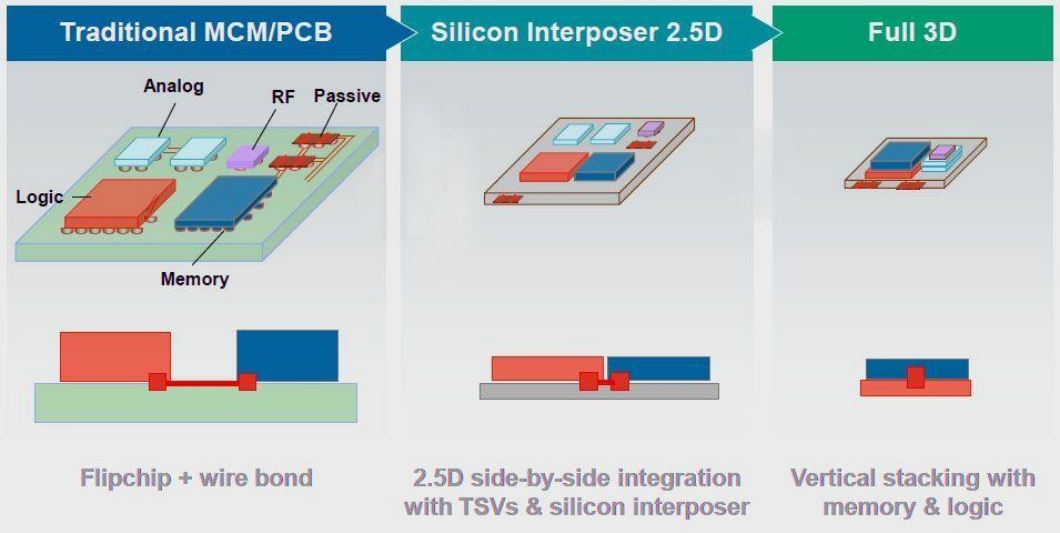
Abstract: Semiconductor companies are integrating multiple dies into a single package. This 2.5D and 3D hybrid integration introduces new ESD challenges but also opportunities.

Introduction

A growing number of semiconductor applications are turning to 2.5D and 3D integration. There are actually various reasons for this trend. Integrating multiple dies in a single package can for instance (1) reduce total power consumption, (2) reduce required PCB area, (3) enhance performance, like higher communication speed and (4) it can speed up development cycles. It also (5) makes it harder for a competitor to copy a chip design/functionality. Finally, (6) it allows to use the most optimal process technology for each function.



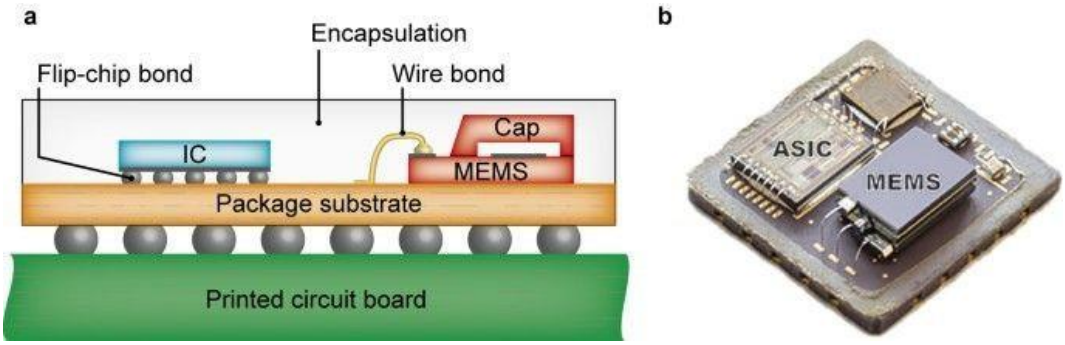
From traditional PCB or MCM approach (left), over 2.5D (middle) to full 3D stacked (right) approach. From https://www.einfochips.com/blog/2-5d-3d-ics-new-paradigms-in-asic/

Whatever the reason for hybrid integration, it is important to consider Electrostatic Discharge (ESD) protection early in the design phase. In the case of packages with a single die, the ESD challenges and solutions have been studied for decades. In that case, designers use (1) foundry provided general purpose I/Os (GPIO) or (2) third party interface IP that already include ESD protection or (3) work with experts to integrate custom ESD solutions. With the advance of 2.5D and 3D integration, there are new ESD challenges but also opportunities for cost reduction.

Example applications

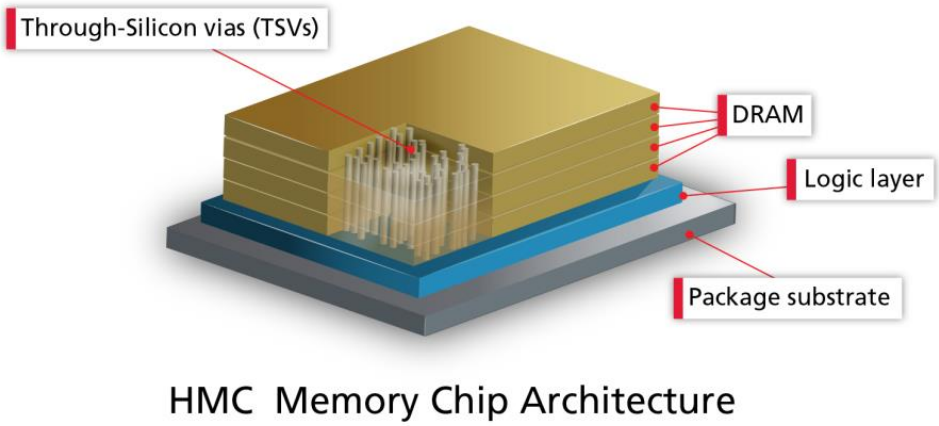
There are already quite some applications that use such hybrid assembly techniques. Chip makers have for instance combined a logic controller chip together with a *Microelectromechanical systems* (MEMS) in one package. This approach has been used for

accelerometers/gyroscope products to reduce the size and volume of the product. Other companies have developed **silicon-based oscillators** to improve the accuracy and flexibility of crystal oscillators. In that case the MEMS is the heart of the oscillator and the logic chip is used to add flexibility like setting different frequencies.



2.5D integration of a logic/CMOS ASIC chip and MEMS accelerometer in one package.
From: https://www.nature.com/articles/micronano20155

One of the typical 3D examples is the **Hybrid Memory Cube** (HMC). In this architecture several DRAM chips are stacked on top of a logic layer. The DRAM chips need a special DRAM process technology (Deep-trench storage capacitor) while the logic layer is built with the most advanced FinFET node. The signals to/from the DRAM layers are sent to the other layers with so-called Through-Silicon Vias (TSV). This has several advantages. The shorter connections allow faster memory access and the 3D stacking also reduces the size/volume of the entire circuit.



Hybrid Memory Chip or Cube architecture. Through-Silicon via's are used for the connections between the logic layer and the DRAM layers.
From: https://community.cadence.com/cadence_blogs_8/b/fv/posts/what-s-new-with-hybrid-memory-cube-hmc

2 types of chip interfaces

For the discussion about ESD we have to clearly define 2 types of chip interfaces.

1. Chip interfaces that connect outside of the package. It could involve bond wires or ball/bumps.
2. Chip interfaces that stay within the package. Different types of connections can be made including wire bonds, flip-chip bonds or through-silicon-via's (TSV) for 3D stacked chips.

For both cases we will discuss the ESD robustness requirements, signal voltage conditions and layout aspects.

ESD robustness

For the first type of interfaces, IC designers have to use the conventional ESD robustness requirements. For most applications that means at least 2kV HBM and about 300 to 500V CDM. There are various applications that have special ESD requirements but that is the scope of another article. For instance, it is quite common to reduce the ESD level (to 1kV HBM, 250V CDM) for wireless interfaces or for high-speed wired communication interfaces. The on-chip ESD protection devices are required to protect against ESD events on the exposed package pins during assembly, transport, testing of the IC product.

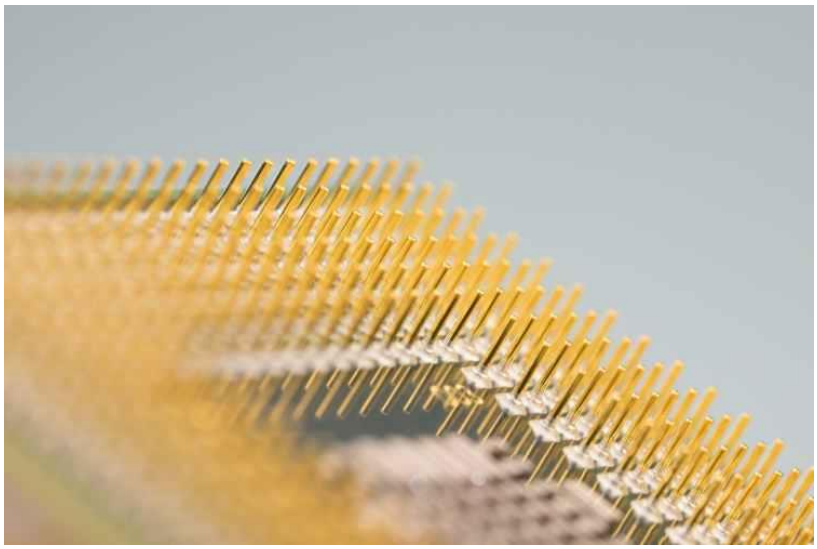


Photo by Pixabay on Pexels.com

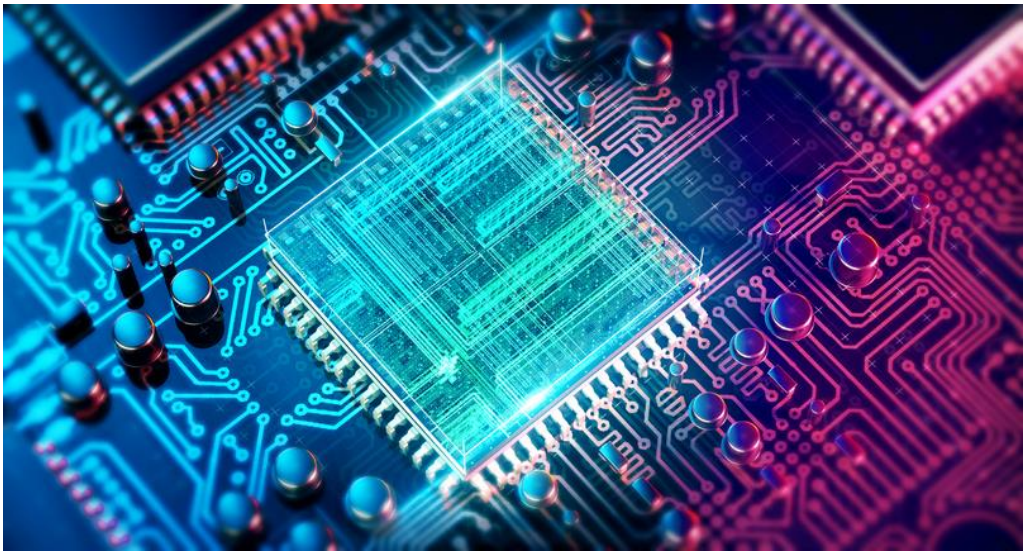
On the other hand, for **chip interfaces that stay inside the package the ESD robustness requirement can be drastically reduced**. Since the connections are not exposed once the IC package is sealed, the likelihood of ESD stress on those lines during IC transport, PCB assembly is strongly reduced. The on-chip ESD devices cannot be completely removed though. ESD events could still occur during the assembly of the different dies inside the package. But such assembly is typically performed under very (ESD) safe/controlled conditions. Actually, the assembly supplier will provide guidelines on minimum ESD requirements.

Examples: Sofics has been involved in several customer engagements for 2.5D and 3D integration projects. For Silicon Photonics the typical HBM level is reduced to 200V or even

100V HBM. For 112Gbps SerDes circuits on chiplets the required ESD protection was set at 35V CDM.

Interface signal voltage

There are always exceptions but for the majority of chip interfaces that connect outside of the package, IC designers can rely on the standard IO library (e.g. 1.8V, 2.5V, 3.3V). Output drivers need to use a high enough voltage and provide large output drive current to ensure the signal can reach the outside of the chip, e.g. charge up the (parasitic) loading capacitance. Usually the functional I/O circuits are built using thick oxide transistors. Typical exceptions are (again) wireless interfaces or high-speed communication lines.

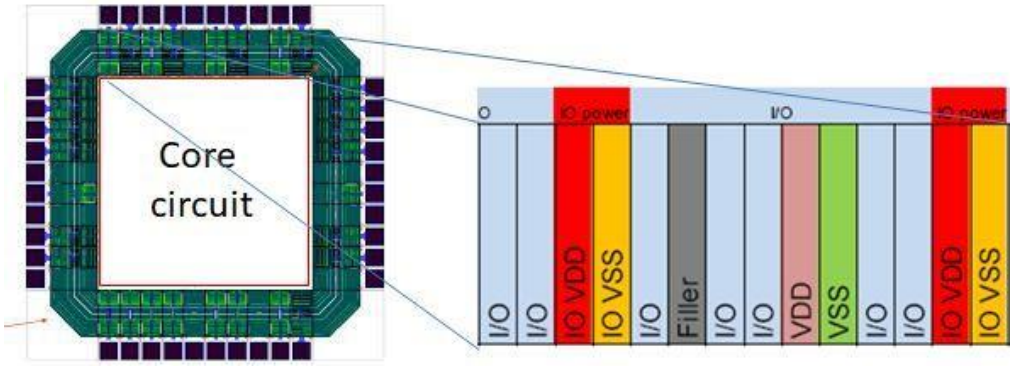


Die-2-die interfaces that stay inside the package do not need high voltage or high drive current capability. The output drivers can be made smaller and can be designed using thin oxide transistors. These transistors are faster but are also more sensitive to ESD events. Typical foundry provided GPIO libraries do not have digital or analog I/O cells for these cases. More effective ESD clamps are needed to protect the sensitive thin oxide transistors and to enable low voltage (1.2V, 1.0V or even lower) operation.

Of course, there are cases where the voltage is actually higher. Some of the applications that involve a combination of logic chips and MEMS actually need a higher output voltage like 5V or 10V, beyond the foundry I/O options.

Layout aspects

Finally, there are several differences for the actual I/O and ESD clamp layout. Interfaces that are connected to the outside of the package are frequently designed into a I/O-ring at the edge of the chip. Foundries provide a set of power/ground pads, digital and analog I/O's, corner and filler cells. IC designers can easily create a custom I/O-ring by combining these different pad-types. Of course, the foundry also provides ESD guidelines on the repetition rate for power pads, minimum number of power pads and the maximum distance for any I/O to a power/ground pad.



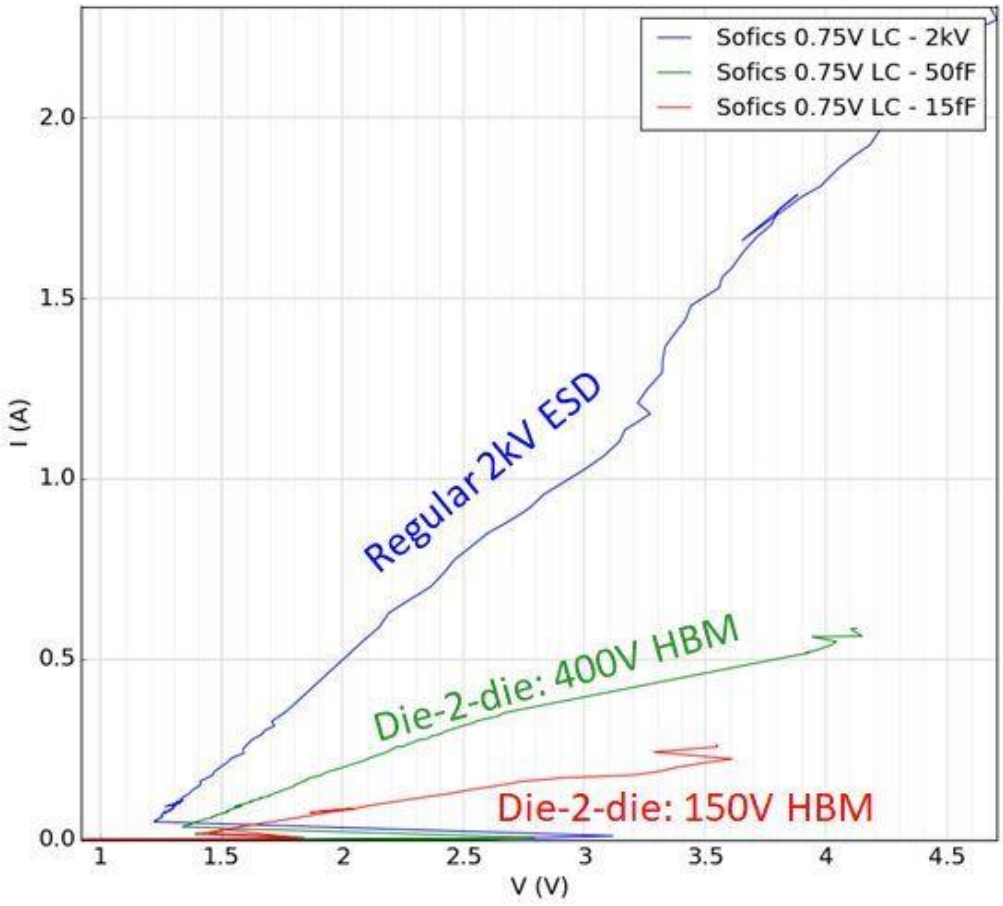
IO-ring circuit

Interfaces that stay inside the package do not really need a complete I/O ring. A small I/O section close to the Through-Silicon Via (TSV) or pad/bump area can suffice. Of course, it is possible to reuse GPIO cells for such an IO section. But there is a great opportunity to reduce silicon area. It is recommended to use custom I/O and ESD cells. These can be smaller and can be designed with a different aspect ratio. It is also recommended to rely on local I/O protection clamps to reduce the need for nearby power protection clamps. More information on local ESD protection is available in a peer-reviewed paper/presentation at the Taiwan ESD and reliability conference (https://www.sofics.com/files/paper/2019-11-TESD-LowcapSerDes.pdf).

Sofics experience

Sofics engineers have been involved in several 2.5D and 3D projects like silicon-based timing products, SerDes on a chiplet and support for improving ESD of a Hybrid Memory Cube. Customized ESD solution libraries (90nm and 65nm CMOS) have been delivered to a CMOS imager company. That company is using 3D stacking to combine a logic chip and the pixel/sensor chip.

ESD protection devices with ultra-low parasitic capacitance have been delivered to more than 15 projects for Silicon Photonics datacenter solutions. In these applications a logic controller, laser and optical die are connected in a single assembly. More information is available in a separate White Paper (https://www.sofics.com/files/whitepaper/on-chip%20ESD%20protection%20for%20SiPho.pdf) .



Example TLP results for Sofics ESD solutions for the protection of interfaces build with thin oxide transistors in 7nm FinFET technology. Three different versions are shown. The blue curve, fit for at least 2kV HBM, can be used for regular interfaces that connect to the outside of the package. The green and red version are a lot smaller and introduce much less parasitic capacitance. These cells have been used to protect die-2-die links in 2.5D Silicon Photonics projects.

Conclusion

ESD protection for 2.5D and 3D packages is different than for regular, single-die packages. IC designers will need customized I/O and ESD solutions because the ESD robustness can be reduced, the signal voltage is outside the standard I/O voltage range, sensitive devices are connected and there is plenty of opportunity to reduce total ESD area.

References, further reading

- More information on ESD aspects can be found in a report from the GSA (Link).
- Local I/O ESD protection approach for high-speed interfaces (https://www.sofics.com/files/paper/2019-11-TESD-LowcapSerDes.pdf)
- Silicon Photonics white paper: https://www.sofics.com/files/whitepaper/on-chip%20ESD%20protection%20for%20SiPho.pdf